

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BOARD OF PATENT APPEALS AND INTERFERENCES**

In Re Application of:	)	
	)	
Ahluwalia, et al.	)	Confirmation No. 1055
	)	
Serial No.: 10/790,509	)	Examiner: Li, Zhuo H.
	)	Group Art Unit: 2185
Filed: March 1, 2004	)	
	)	
For: <b>Memory Management</b>	)	HP Docket No.: 200315654-1
	)	TKHR Docket No.: 050849-1450
	)	

**REPLY BRIEF**

This brief is filed in reply to the Examiner's Answer, which was mailed October 2, 2009.

**Response to Examiner's Answer**

The rejection sections on pp. 3-12 of the Examiner's Answer appear to generally recapitulate the prior positions taken by the Examiner in the final Office Action. Appellant continues to disagree with the Examiner's positions as to all claim rejections under appeal, and Appellant's Appeal Brief sets forth substantive reasons why the references of record do not properly teach the claimed features. Appellant addresses herein selected points that were introduced in the Response to Arguments section of the Examiner's Answer (pp. 12-35).

**Rejection of claim 23 under 35 U.S.C. § 112, ¶1 (written description)**

The Examiner's Answer alleges (p. 13) that "appellant admitted in Appeal Brief (page 8) that the instant specification *only* defines computer readable medium as including any medium that can store or transfer information" (emphasis in original). Appellants disagree: Appellant's admission did not extend to saying that the discussed definition is the "only" definition.

The Examiner's Answer further alleges (p. 13) that "it is notoriously well known in the art that **computer readable medium** is a broad term in accordance with plain meaning that **includes** any type of memory devices, **as well as signals or carrier waves** such that any type of memory devices, as well as signals or carrier waves can store and transfer information".

Appellant first disagrees with the contention that a person of ordinary skill in the art would understand “computer readable medium” to include signals or carrier waves, and submits that the Examiner has merely made a conclusory statement that this is so, unsupported by evidence or reasoning. The Examiner’s rationale for the written description rejection appears to be: because the specification does not show the inventors had possession of signals storing computer instructions, the inventors did not have possession of a computer readable storage medium storing computer instructions. Appellant submits that this rejection is premised upon a faulty interpretation of “computer readable storage medium”, and should therefore be overturned. Appellant also submits that the Examiner’s broad reading of “computer readable medium” is irrelevant to whether or not the inventors possessed a storage medium.

As argued in the Appeal Brief (p. 9), “storage medium” is clearly understood, as a matter of plain English, to be a particular type of computer readable medium, one that stores computer readable instructions. The instant specification (para. 0024) states that: “A computer readable medium may include any medium that can store or transfer information.” In view of this evidence that the inventors did possess a “computer readable storage medium”, the Examiner’s *prima facie* case for a written description rejection is deficient, and the rejection should be overturned.

**The transient flag in Browning does not correspond to an indication...that the virtual address space, previously available to the process, is no longer valid**

A fundamental point of disagreement between Appellant and the Examiner relates to how *Browning* allegedly teaches an indication that the virtual address space is no longer available to the process (as found in claims 1, 8, 19, 22, and 23, with some variations). Appellants have explained in three previous responses why various teachings and data structures in *Browning* do not correspond to the claimed indication.

The Examiner’s Answer appears to set forth a new allegation about the claimed indication, namely that *Browning*’s transient flag corresponds to the claimed indication:

...Note Browning also teaches that the pre-translations are stored in an RPN list which is stored with the buffer memory descriptor (col. 7 lines 15-16) and a transient flag is set in the buffer descriptor for determining whether virtual memory is removed in progress (col. 7 line 50 through col. 8 line 44). Thus, the RPN list as taught by Browning can be considered as the virtual memory data structure, and the ***transient flag as taught by Browning can be read on the claimed limitations of "indication*** in a virtual memory data structure associated with the process that the virtual address space, previously available to the process, is no longer valid". (Examiner's Answer, p. 15.)

Appellant submits that such a change in position amounts to a new ground of rejection, although the Examiner did not identify it as such. Although Appellant is entitled an opportunity to reopen prosecution to properly address this new ground, Appellant chooses not to exercise this right, and instead chooses to move forward with the appeal. Appellant now addresses the newly-relied-upon teaching in *Browning* that was introduced in the Examiner's Answer.

Simply put, *Browning* does not teach that the transient flag describes whether virtual memory is "removed in progress", as specifically alleged by the Examiner. Nor does *Browning* teach that the transient flag describes whether virtual address space is no longer available to the process, as claimed. Instead, *Browning* teaches that the transient flag describes whether an RPN list is expected to be used by one I/O operation or by multiple I/O operations:

A bit is stored in field 60 that indicates whether the RPN list 58 is transient. The list is transient when it is expected to be used only once, e.g. when there is only one expected I/O operation using this list. The list is not transient when it is expected to be used multiple different times for many I/O operations.  
(Col. 5, lines 45-50.)

Appellant submits that this is not the same as that an indication that the virtual address space is no longer available to a process, as claimed. Furthermore, the Examiner has provided no explanation as to why an indication of the number of I/O operations that are expected to use an RPN list would be understood by a person of ordinary skill in the art to be an indication that virtual address space is no longer available to a process.

Because the Examiner's Answer clearly and specifically alleges that the transient flag corresponds to the claimed indication (p. 15, lines 16-21), Appellants submit that the Examiner

has, by implication, withdrawn the previous allegations about *Browning*'s memory-move-in-progress flag corresponding to the claimed indication. However, if the Board chooses to consider the Examiner's previous allegations about the in-progress flag, a discussion of the in-progress flag, and its deficiencies in disclosing the disputed claim language, was previously set forth in the Appeal Brief (see, e.g., section VII.B.1.a.(2)).

**The RPN in *Browning* does not correspond to a virtual memory data structure for a process**

Another fundamental point of disagreement between Appellant and the Examiner relates to how *Browning* allegedly teaches that the indication described above is located in a virtual memory data structure for a particular process (as found in claims 1, 8, 19, 22, and 23, with some variations). Appellants have explained in several previous responses why various data structures in *Browning* are not part of a virtual memory data structure for a process

In the Examiner's Answer, the Examiner appears to provide a new explanation (p. 15) for why the RPN list allegedly resides in a virtual memory data structure: "Browning also teaches that the real page number (RPN) list includes pre-translations for a particular set of virtual addresses so that **each RPN list includes a list of different set of virtual addresses**". Appellant submits that such a change in position amounts to a new ground of rejection, although the Examiner did not identify it as such. Although Appellant is entitled an opportunity to reopen prosecution to properly address this new ground, Appellant chooses not to exercise this right, and instead chooses to move forward with the appeal. Appellant now addresses the newly-relied-upon teaching in *Browning* that was introduced in the Examiner's Answer.

Appellant assumes (for the sake of argument) that the RPN list is a virtual memory data structure. Even so, the fact that different RPN lists include different sets of virtual addresses does not imply that the RPN list is per-process (*i.e.*, associated with one particular process). Nor has the Examiner provided any explanation as why the existence of different sets of virtual

addresses within RPNs would be understood by a person of ordinary skill in the art as a per-process RPN.

The Examiner further alleges (p. 16) that because a flag is stored in a buffer descriptor which is stored with an RPN list, “the flag has affect a particular process”. Appellant disagrees. The Examiner has not pointed to any portion of *Browning* that describes a buffer descriptor as per-process. Furthermore, as noted above, the Examiner has not convincingly explained why the RPN list in *Browning* would be considered to be per-process.

**Moving real pages of memory in *Browning* does not correspond to release of physical address space**

Another fundamental point of disagreement between Appellant and the Examiner relates to how *Browning* allegedly teaches detecting that physical address space has been released (as found in claims 1, 8, 19, 22, and 23, with some variations). Appellants have explained in several previous responses why various actions in *Browning* do not correspond to this claimed feature.

The Examiner’s Answer (p. 18) maintains the position that “the teaching of *Browning* removal of real pages of memory (col. 9 lines 4-10) [reads on] the claimed limitation of release of physical address space”. However, the Examiner did not address the point made in the Appeal Brief (see, e.g., section VII.B.1.b.(2)) that *Browning* does not actually teach removing or releasing physical address space, but instead teaches relocating pages from one physical address to the other. Appellant submits that relocating pages in physical memory is not the same as releasing pages since the pages are still in use. Nor has the Examiner rebutted Appellant’s explanation (in the same section of the Appeal Brief) that *Browning* does not teach detection of the alleged “removal of real pages of memory”, much less an indication triggered by such detection.

Moreover, it appears that the Examiner is relying on a combination of different aspects of *Browning* for teaching the claims at issue:

- release of physical address space -> relocating pages in real memory
- detection -> checking memory-move-in-progress flag or transient flag
- indication -> setting memory-move-in-progress flag or transient flag

However, these features are not claimed in isolation, but are interrelated in a specific way.

Namely, the release of physical address space is detected, and this detection triggers an indication in a particular data structure. Even assuming (for the sake of argument) that relocation of real pages, checking a flag, and the presence of a flag corresponds to release of physical memory, detection, and indication, these features are not related in *Browning*: checking one of these flags has nothing to do with detecting release of physical address space; and setting one of these flags has nothing to do with detecting release of physical address space. Nor has the Examiner explained why a person of ordinary skill in the art would modify *Browning* to couple the release of physical address space to the use of these flags.

Respectfully submitted,

By: /Karen G. Hazzah/

Karen G. Hazzah,  
Reg. No. 48,472

**THOMAS, KAYDEN, HORSTEMEYER  
& RISLEY, L.L.P.**  
600 Galleria Parkway, NW  
Suite 1500  
Atlanta, Georgia 30339-5948  
Tel: (770) 933-9500  
Fax: (770) 951-0933